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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/534,329	05/09/2005	Royce Lowis	GB02 0188 US	2947

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EXAMINER	
KALAM, ABUL	

ART UNIT	PAPER NUMBER
2814	

NOTIFICATION DATE	DELIVERY MODE
11/16/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/534,329	LOWIS, ROYCE	
	Examiner	Art Unit	
	Abul Kalam	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2007 to 17 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/9/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group I, claims 1-5, in the reply filed on June 21, 2007, is acknowledged. Because applicant did not distinctly and specifically point out any errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Furthermore, note that claims 6-10 were cancelled, and thereby, claims 1-5 remain pending in the Application.

Claim Objections

2. Claims 2-5 are objected to for the following reasons:

In line 1 of claims 2-5, the limitation of "A semiconductor device," should be amended to --The semiconductor device--, because the limitation refers to a feature already claimed.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1-5** are rejected under 35 U.S.C. 102(b) as being anticipated by **Daily et al. (US 4,729,006; hereinafter, Daily)**.

Regarding **claim 1**, Daily teaches a semiconductor device (FIG. 1) comprising:

a semiconductor substrate (10, FIG. 1) of first conductivity type (P-type; col. 5, lns. 33-35: "the substrates may have either a P or N conductivity") having opposed first and second major surfaces;

a semiconductor component (P-type channel transistor formed in region 22, FIG. 1) defined adjacent to the first major surface (26, FIGs. 1 and 2B);

a trench (12, FIG. 1) extending from the first major surface into the semiconductor substrate, having an inner side (18) facing the semiconductor component (P-type channel transistor) and an outer side (20, FIG. 1) opposed to the semiconductor component;

a thermal oxide (52 and 32, FIG. 1; col. 8: lns. 49-66) filling the trench (12, FIGs. 2C-2E); and

a channel stop diffusion (40, FIG. 1; col. 9, lns. 54-57) of first conductivity type (P-type) extending from the first major surface (26) on the outer side (20, Fig. 1) of the trench (12) and further extending under the trench from the outer side to the inner side of the trench (Fig. 1).

Regarding **claim 2**, Daily teaches the semiconductor device (FIG. 1) according to claim 1, further comprising a well (N-well; col. 8: lns. 21-31) of a second conductivity type (N-type) opposite to the first conductivity type (P-type), implanted into the first major surface (26) of the semiconductor substrate (10, FIG. 2B); wherein the trench (12) extends from the first major surface (26) through the well (N-well) into the substrate (10, FIGs. 1 and 2B).

Regarding **claim 3**, Daily teaches a semiconductor device (FIG. 1) according to claim 2, wherein the semiconductor component is a first transistor (P-type channel transistor, FIG. 1), the semiconductor device further comprising:

a second transistor (N-type channel transistor formed in region 24, FIG. 1) adjacent to the first transistor;

a second trench (13, FIG. 1) around the second transistor (N-type channel transistor) extending from the first major surface (26) into the semiconductor substrate (10), having an inner side (21) facing the second transistor and an outer side opposed to the second transistor; and

a thermal oxide (52 and 32, FIG. 1; col. 8: lns. 49-66) filling the second trench (13, FIGs. 2B, 2D, 2E);

wherein the channel stop diffusion (40, 42, FIG. 1) extends from the first major surface (26) between the first and second trenches (12, 13) and under each of the first and second trenches (12, 13).

Regarding **claim 4**, Daily teaches a semiconductor device (FIG. 1) according to claim 1, wherein the semiconductor component (P-type channel transistor) is an insulated gate field effect transistor (col. 9: lns. 28-65) having longitudinally spaced source and drain implants ("source and drain regions," col. 9: lns. 58-60) in the well (N-well, FIG. 1) defining a channel region at the first major surface (26) between the source and drain implants.

Regarding **claim 5**, Daily teaches a semiconductor device (FIG. 1) according to claim 4, comprising a gate oxide (76, FIG. 1) over the channel region of the first major

(26) surface and a gate (78) over the gate oxide (76), wherein the gate oxide (76) and gate (78)span the channel region from the trench on one side of the channel region to the trench on the other side of the channel region so that the channel region extends laterally between the trenches (col. 9: lns. 35-45; it is implicit that the channel region extends laterally between the trenches).

4. **Claim 1** is rejected under 35 U.S.C. 102(b) as being anticipated by **Liou et al. (US 5,130,268; hereinafter, Liou)**.

Regarding **claim 1**, Liou teaches a semiconductor device (FIG. 1f) comprising:

a semiconductor substrate (2, FIG. 1f) of first conductivity type (P-type; col. 3: lns. 48-65) having opposed first and second major surfaces;

a semiconductor component ("transistors," col. 6: lns. 66-68) defined adjacent to the first major surface (20n or 20p, FIG. 1f);

a trench (10, FIG. 1b; col. 4, lns. 46-64) extending from the first major surface into the semiconductor substrate (2), having an inner side facing the semiconductor component and an outer side opposed to the semiconductor component ("transistors," col. 6: lns. 66-68);

a thermal oxide (16, FIG. 1f; col. 6, lns. 9-20) filling the trench (10); and

a channel stop diffusion (FIG. 1f; col. 4, lns. 65-68) of first conductivity type (P-type, col. 5: lns. 3-21) extending from the first major surface on the outer side of the trench (10, FIG. 1b) and further extending under the trench from the outer side to the inner side of the trench (10, FIG. 1b).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is 571-272-8346. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. K./

/Phat X Cao/
Primary Examiner, Art Unit 2814